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SC12866TP

PTO/SB/08A (04-03)

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Sheet	1	of	1
		Application Number	10/662832
		Filing Date	
		First Named Inventor	Michael J. Rendon et al.
		Group Art Unit	2818
		Examiner Name	
		Attorney Docket Number	SC12866TP

U. S. PATENT DOCUMENTS					
Examiner Initials ¹	Cite No. ¹	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number -Kind Code ² (if known)	MM-DD-YYYY		
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NON PATENT LITERATURE DOCUMENTS					
Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ²
EJ	AM	VAN MEER, Hans et al.; "70 nm Fully-Depleted SOI CMOS Using a New Fabrication Scheme: The Spacer/Replacer Scheme"; Symposium on VLSI Technology Digest of Technical Papers; 2002; 2 pp; IEEE			

Examiner Signature	B. J.	Date Considered	9-10-04
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